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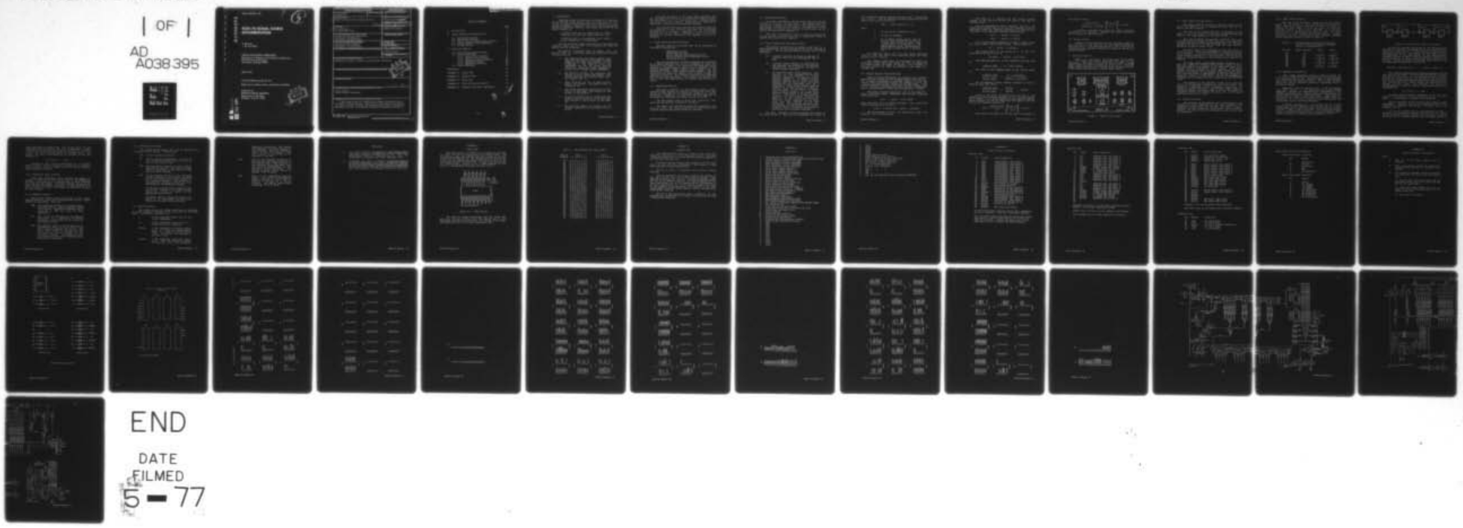

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BCSG-76 SIGNAL SOURCE DOCUMENTATION

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This memo serves to document the design and operation of the BCSG-76 signal source. This unit is the latest in a series of signal sources designed and constructed at Cooley Electronics Laboratory for use in performing acoustic propagation studies.

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TABLE OF CONTENTS

A

1. Introduction

This memo serves to document the design and operation of the BCSG-76 signal source. This unit is the latest in a series of signal sources designed and constructed at the Cooley Electronics Laboratory (CEL) for use in performing acoustic propagation studies. The signals generated by the BCSG-76 consist of

> a carrier that can be amplitude or phase modulated by a periodic binary sequence, and
>
> a waveform that is constructed from sample values scanned out of a ROM memory

The only external signal required is a clock waveform symmetric about its dc level at a frequency 64 times the desired carrier frequency.

The BCSG-76 is modeled after an earlier unit, the BCSG-74 (Ref. 1). The major external differences between the two units are

1. The BCSG-76 does not have a phase lock loop and thus must be furnished a timing signal at 64 times the desired carrier frequency. The BCSG-74 unit can synthesize its own 64 times carrier reference using an input waveform at carrier or at 4 times carrier frequency.

2. The BCSG-76 accepts its sequence law setting in octal rather than binary. This allows ready use of existing tables (see, for example, Ref. 2).

3. Digit durations of up to 999 carrier cycles are allowed. The BCSG-74 unit is limited to 99.

4. The binary modulating sequence can be read from a 32 word ROM. This feature is not present in the BCSG-74.

5. An analog waveform can be synthesized from sample values stored in a 64 word ROM. This feature is not present in the BCSG-74.

6. The maximum number of stages in the sequence generator was increased from 12 to 14.

With the exception of the clock input amplifier and the D/A converters, the unit is constructed using TTL logic. The electronics are all contained on a commercially available wire-wrap panel. Duplication or modification should be a relatively straightforward process.

The following sections describe the waveforms that can be produced by the BCSG-76 and how the controlling parameters are entered. Appendices A and B contain descriptions of the ROM's. Appendix C has a parts list, Appendix D, cabling information, and Appendix E, a set of diagrams.

2. Output Waveform Characteristics

The five types of waveforms that can be generated by the BCSG-76 consist of:

unmodulated carrier
ROM stored waveform
binary sequence AM modulated carrier
binary sequence phase modulated carrier
AM pulsed carrier

The carrier/waveform clocking frequency is controlled by an input waveform that is at a frequency 64 times that desired at the output. All waveforms are generated using counters to address ROM's, which contain "samples" of the desired waveforms. These samples are loaded into D/A converters where they become analog signals. The D/A converters are wired to accept 8-bit values using 2's complement notation. The resulting waveforms are quantized both in time and amplitude. The output waveforms are unfiltered and swing between a nominal plus and minus 5 volts.

2.1 Unmodulated Carrier

The carrier waveform is generated using a 6-bit (divide by-64) counter to address a 64-word by 8-bit ROM. Stored in this ROM are the quantized values of a cosine waveform. Appendix A describes how this ROM unit is organized and tabulates the values stored in the ROM.

The ROM outputs feed an 8-bit D/A converter that generates the desired "continuous" waveform.

The pulse, AM, and phase modulated waveforms are derived from this carrier waveform by selectively using up/down counting and on/off gating as required.

2.2 ROM Stored Waveform

A second, independent, divide by-64, ROM unit and D/A converter cluster is provided. The output from this collection is always available and is not affected by any of the control settings on the BCSG-76. The ROM used in this application is organized in exactly the same manner as the cosine ROM described in Appendix A.

This unit is provided in order to allow the generation of any periodic waveform that can be represented using 64 equally time spaced 8 bit samples.

2.3 Binary Sequence AM Modulated Carrier

The carrier waveform can be gated on and off in a manner determined by the settings of the panel controls on the BCSG-76. The controlling waveform can be one of three waveforms:

a) A binary sequence of length up through 32 digits that has been programmed into a ROM.

b) A binary linear sequence as determined by the sequence law entered in the switches provided for this purpose (usually a linear maximal sequence).

c) An augmented binary linear sequence. This feature is only intended for use with sequence laws corresponding to linear maximal sequences. An augmented linear maximal sequence is a linear maximal sequence that has had an extra zero added changing the n-1 zero-tuple into an n zero-tuple. Since linear maximal sequence lengths are 1 digit short of being an integer power of two digits in length, this feature results in a periodic sequence whose length is an integer power of two. Extending a linear maximal sequence in this manner affects the spectrum of the resulting waveform. However, "good" sequences can be found such that this effect is not too disruptive. The advantage gained by such an extension is the ability to use "fast" discrete Fourier transform algorithms in processing the resulting receptions.

Let b(t) represent a binary waveform that takes on the values Ø and 1. The value Ø corresponds to a "zero" in

the controlling binary sequence and the value 1 corresponds to a "one". The AM modulated waveform generated by the BCSG-76 unit can be written as

$$s(t) = 5\, b(t) \cos(2\pi\, ft + a)$$

where

f is the carrier frequency in Hz.

t is time in seconds.

a is a phase angle which can be entered into the BCSG-76 as 64ths of a cycle using octal notation. This corresponds to being able to set 360/64 degree steps. The setting is described in more detail in Section 2.4.

The amplitude factor of 5 in the above equation results from the use of D/A converters which can swing between +5 and -5 volts.

The sequence generator is designed so that the durations of the "ones" and "zeros" in b(t) correspond to an integer number of cycles of carrier. The number of carrier cycles per digit is settable in the range of 1 through 999.

2.4 Binary Sequence Phase Modulated

Rather than AM modulating the carrier, the available sequences can instead be used to phase modulate the carrier. For a sequence containing a balanced number of "ones" and "zeros" this effectively doubles the average power in the resulting waveform without affecting the peak power. This is an important consideration since acoustic transducers tend to be peak power, rather than average power, limited.

The method of phase modulation used in the BCSG-76 is termed "conjugate phase" modulation and involves assigning phase angles as

$$a(t) = (2b(t) - 1)*2\pi *N/64$$

where the value of N is switch settable. The resulting output waveform can be written

$$s(t) = 5 \cos\{2\pi\, [ft + (2b(t) - 1)*N/64]\}$$

The transitions of b(t) are phased so that the waveform, s(t), is continuous.

The value of N controls how the signal energy divides in the spectrum between the carrier line and the sideband lines.

For the nonaugmented linear maximal sequence the energy split between the carrier and the sidebands is easily determined using the baseband equivalent correspondences (assuming a unit amplitude baseband representation)

$$\text{"zero"} = \cos(a) - j \sin(a)$$

$$\text{"one"} = \cos(a) + j \sin(a)$$

In a linear maximal sequence of length L digits there are (L+1)/2 "ones" and (L-1)/2 "zeros". The dc level is

$$\text{dc} = \cos(a) + j \sin(a)/L$$

The average power in one period is 1. Of this the contribution by the dc line is

$$\text{dc power} = \cos^2(a) + \sin^2(a)/L^2$$

The remaining power is in the sidebands and must then be

$$\text{sideband power} = (1 - 1/L^2) \sin^2(a)$$

The ratio of the sideband power to the carrier power is

$$\frac{\text{sideband power}}{\text{carrier power}} = \frac{(1 - 1/L^2)\sin^2(a)}{\cos^2(a) + \sin^2(a)/L^2}$$

For an augmented linear maximal sequence a similar analysis gives the result

$$\frac{\text{sideband power}}{\text{carrier power}} = \frac{\sin^2(a)}{\cos^2(a)} = \tan^2(a)$$

Given a periodic waveform with period T, the associated power spectrum consists of a set of lines spaced 1/T Hz apart. For a phase modulated linear maximal sequence based waveform, it can be shown that the power in the kth line of the baseband waveform is

$$P(k) = \frac{\sin^2(a)*(L+1)}{L^2} \left[\frac{\sin(k \pi L)}{k \pi L}\right]^2, \text{ k not } 0$$

The ratio of the power in the kth line to the power in

the carrier line is

$$\frac{\sin^2(a) * (L+1)}{L^2 * \cos^2(a) + \sin^2(a)} \left[\frac{\sin(k \pi L)}{k \pi L}\right]^2, \; k \text{ not } 0$$

A similar expression for augmented linear maximal sequences is not possible. However, the above expression can be used as an approximation.

2.5 Pulsed Carrier

Instead of being modulated by the available sequence, the carrier can be gated on for one digit duration per sequence period. Both the phase angle at which the carrier is turned on and the digit duration in cycles of carrier are switch settable.

3. Using the BCSG-76

Figure 1 is a drawing of the front panel of the BCSG-76. All input and output connections are made via BNC connectors. The power is turned on and off using a toggle switch mounted on the left-hand side of the unit. Three LED power supply indicators are mounted above the power switch. A dim or dark LED indicates a faulty power supply.

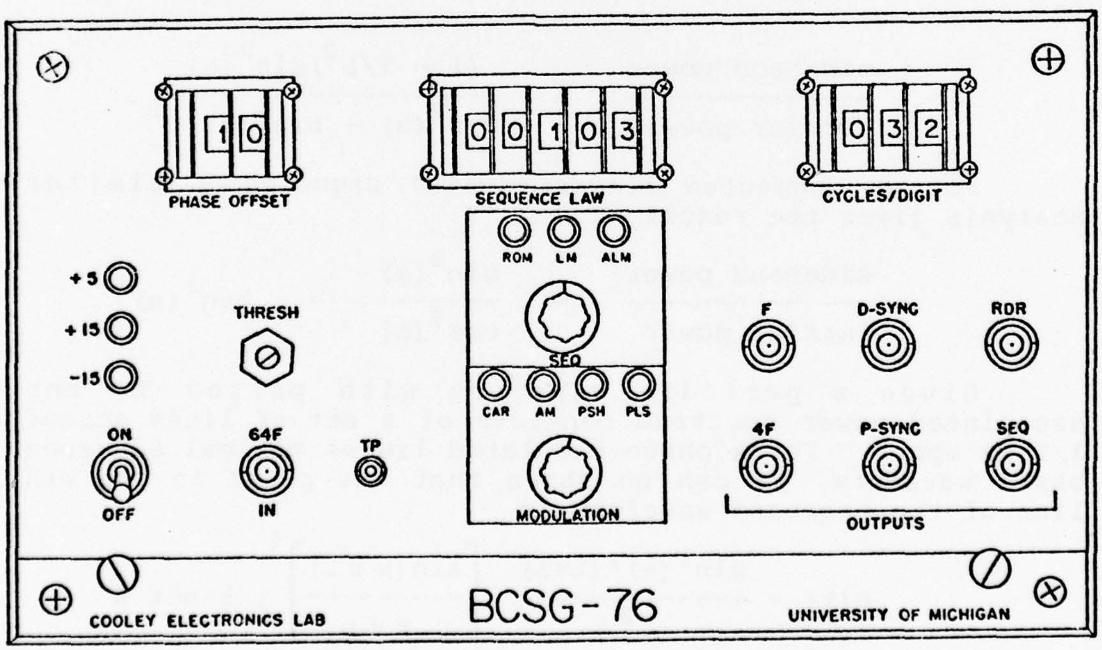


Figure 1. BCSG-76 front panel

3.1 Clock Input Characteristics

The input waveform should be symmetric about its dc level and should be at a frequency 64 times that of the desired carrier frequency.

The input is ac coupled and has an impedance of 10k ohms. The 3 dB points on the input signal conditioning amplifier are approximately at 8 Hz and 100 kHz.

With the threshold adjustment properly set, the clocking circuitry begins to work when the signal amplitude is approximately 0.25 volts peak-to-peak (pp). For reliable operation in the 8 Hz to 100 kHz range the input waveform should be no smaller than 1 V pp.

The upper limit on the frequency of the input clock is on the order of 1 MHz (corresponding to a carrier frequency of 15.625 kHz). To attain this limit, the amplitude of the input waveform should be 3 v pp or greater. This frequency limit is imposed by delays in the clocking logic used in the BCSG-76.

The input clock conditioning circuit consists of a gain of 5 amplifier feeding a TTL Schmitt trigger circuit. The input signal is ac coupled to the amplifier where it is summed with an adjustable offset voltage. This offset voltage is used to shift the zero input signal operating point to the middle of the Schmitt trigger's input range. This operating point is appropriate if the input waveform is symmetic around its dc level. The use of nonsymmetric waveforms can be compensated for by resetting the threshold level.

The waveform at the amplifier output can be observed using an oscilloscope connected to the TP tip jack. The amplifier is designed so that negative excursions are clipped at about -0.6 volts. The Schmitt trigger input is protected against excursions above +5 volts. To adjust the threshold setting for normal operation, set the dc level measured at TP to +1.3 volts.

3.2 Selector Switches

The operation of the BCSG-76 unit is controlled by the settings of three thumbwheel and two rotary switches. The thumbwheel switches are used to enter the phase offset, sequence law and cycles per digit count. The two rotary switches are used to select the sequence source and the type of modulation.

3.2.1 Phase Offset Selector

This two digit thumbwheel switch controls the phase angle of the carrier at which modulating transitions are made. When AM or pulse modulation is used, this setting selects the phase angle at which the carrier is gated on. When the carrier is being phase modulated, this setting selects the +- angle excursion that is used. The angle setting is in octal allowing 64 possible angles. Common settings and the corresponding unit amplitude baseband signal representations are given in Table 1.

Table 1. Correspondence between phase setting, carrier transition angle and baseband "zero-one" representation

Setting	Angle (degrees)	"Zero"	"One"
00	0	1	1
10	45	$(1-j)/\sqrt{2}$	$(1+j)/\sqrt{2}$
20	90	$-j$	$+j$
30	135	$(-1-j)/\sqrt{2}$	$(-1+j)/\sqrt{2}$
40	180	-1	-1
50	-135	$(-1+j)/\sqrt{2}$	$(-1-j)/\sqrt{2}$
60	- 90	$+j$	$-j$
70	- 45	$(1+j)/\sqrt{2}$	$(1-j)/\sqrt{2}$

3.2.2 Sequence Law Selector

This 5 digit thumbwheel switch is used to select the "law" to be followed by the non-ROM periodic binary sequence that modulates the carrier. Sequence laws are entered using the octal notation described below. The 5 octal switches permit the use of sequence generators containing from 2 through 14 stages.

Reference 2 can be consulted for a list of sequence laws that result in the generation of maximal length sequences. Because of implementation considerations, the sequence generated from a given setting is actually the so-called reverse sequence (described below). This should be accounted for when writing processing programs that are sensitive to the exact sequence law governing the transmission (e.g., multipath programs).

A common technique for the generation of random appearing binary sequences involves the use of a logic circuit made up of flip-flop delay stages and exclusive-or circuits. While many "canonical" interconnection schemes exist, a particularly useful one is termed the modular shift register generator, schematically diagrammed in Fig. 2.

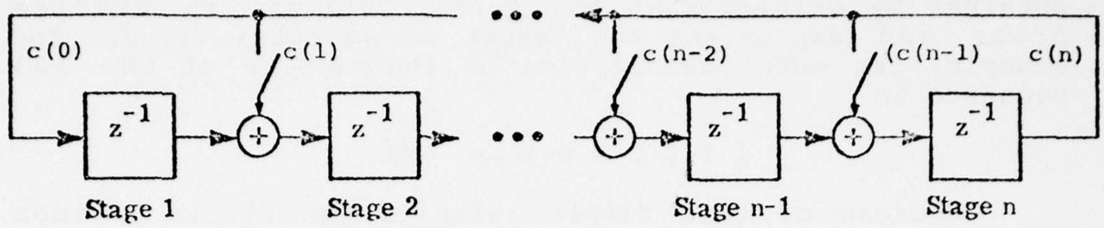


Figure 2. Modular shift register generator

The switch settings represented by the constants c(0) through c(n) determine the properties of the binary sequence generated by this circuit. In the case of the modular shift register generator, the switch settings have a 1-to-1 correspondence to the coefficients in the characteristic polynomial which is used to desribe sequences generated by circuits made up of delay flip-flops and exclusive-or circuits. Given a generator of the type shown in Fig. 2 the corresponding characteristic equation is

c(n)*z^n + c(n-1)*z^(n-1) + ... + c(1)*z + c(0) = 0

The indicated additions are performed modulo-2 and the c(i) take on the value 1 if the associated switch is closed and take on the value of 0 if the associated switch is open. Because the values that the c's can take on are restricted to 0 and 1, a convenient shorthand notation involves writing the coefficients as a binary number and expressing this number in octal form. For example, the generator corresponding to c(6)=c(1)=c(0)=1, c(5)=c(4)=c(3)=c(2)=0 is represented by

1 0 0 0 0 1 1 = 103

A linear maximal sequence generator is one that will generate a string of 1's and 0's whose period is L = 2^n-1 where n is the number of stages in the generator.

Not all possible switch settings yield maximal length sequences. Various tables are available which can be consulted to determine the proper settings (see, for example, Ref. 2).

If it were possible to run the generator of Fig. 2 backward, the resulting sequence would be the time reverse of the sequence obtained running the generator forward. Obviously if the forward sequence were of maximal period so

would the reverse sequence be. The octal form of the characteristic equation of the reverse sequence is easily obtained by writing down the switch settings in reverse order and expressing the result as an octal value. For example, the octal description of the reverse of the 103 sequence is

1 1 0 0 0 0 1 = 141

Because of this simple relationship it is common practice not to include reverses in tabulations of sequence laws. Usually, only the member with the lower numeric representation is listed.

3.2.3 Cycles per Digit Selector

This three thumbwheel switch controls the number of cycles of carrier making up a digit in the modulating waveform. This setting is in decimal and is often referred to as the Q of the signal. The digit duration can be set at from 1 through 999 cycles of carrier. A digit duration of 0 cycles of carrier yields a CW output but should not be used for this purpose.

3.2.4 Sequence Selector

This rotary switch selects the source of the binary sequence which is to be used to modulate the carrier. Three choices are available. These are:

ROM The modulating sequence is scanned from a read only memory. Maximum sequence length is 32 digits. Appendix B describes how to organize a ROM for use in this application.

LM The carrier is modulated by the sequence generated by a sequence generator connected as determined by the sequence law switch setting.

ALM The sequence used in the LM position is augmented by adding an extra "zero" digit and is used to modulate the carrier. The extra "zero" digit is inserted into the (n-1)-tuple of zeros present in the original sequence. The augmenting will not necessarily work if the sequence being generated is nonmaximal.

3.2.5 Modulation Selector

This rotary switch selects the type of modulation to be applied to the carrier. Choices are:

CAR Carrier without modulation

AM On-off amplitude modulation. A "zero" in the governing sequence turns the carrier off, a "one" turns it on.

PHS The controlling sequence is used to phase modulate the carrier. The amount of phase shift is determined by the setting of the phase selector switches.

PLS If the sequence source is the internal sequence generator, the carrier is gated on for one digit duration per period of the selected sequence. The period of a non-augmented sequence is one less than the period of the augmented sequence.

If the ROM is being used to generate the controlling sequence, the digits during which the carrier is gated on are programmed into the ROM.

The phase angle at which the carrier is gated on is determined by the value entered in the phase offset switches.

3.3 Output Waveforms

The output timing and signal waveforms are available on 6 BNC connectors located on the right side of the front panel. The signals available are:

F A TTL compatible square wave at the carrier frequency.

4F A TTL compatible square wave at 4 times the carrier frequency.

D-SYNC A TTL compatible positive going pulse of duration approximately equal to 1 cycle of the 64F input clock. The pulses are provided at the digit rate.

P-SYNC A TTL compatible positive going pulse. When the modulation source is derived from the internal

sequence generator, this pulse corresponds to one digit duration of the sequence. When the modulation source is from the sequence ROM, this pulse is controlled by the contents of the ROM.

RDR — This is the waveform produced by scanning the auxillary 64-word by 8-bit waveform ROM. This waveform is only affected by the 64F input clock and operates independently of the selector switch settings. The nominal maximum output swing is between -5 to +5 volts.

SEQ — This is the modulated carrier output. The carrier is synthesized using a 64-word by 8-bit ROM to contain 1 period of a cosine waveform. The nominal output swing is between -5 to +5 volts.

References

1. F.J. Looft, BCSG-74: An Augmented Linear Maximal Shift Register Sequence Generator, Cooley Electronics Laboratory Technical Memorandum No. 110, The University of Michigan, Ann Arbor, September 1975.

2. K. Metzger, Jr. and R. J. Bouwens, An Ordered Table of Primitive Polynomials Over GF(2) of Degrees 2 Through 19 for Use With Linear Maximal Sequence Generators, Cooley Electronics Laboratory Technical Memorandum No. 107, The University of Michigan, Ann Arbor, July 1972.

APPENDIX A

Cosine ROM

The ROM's used in the BCSG-76 are Signetics type 8223 or 82S23 which are organized as 32 8-bit words. The manufacturer names the address pins AØ through A5 and the output pins BØ through B7. The convention used in the BCSG-76 has the bit significance going from least to most as the associated numbers go from Ø up. A high level corresponds to a logical one. Figure A-1 is a logic diagram of the 82(S)23. Unprogrammed locations contain "zeros".

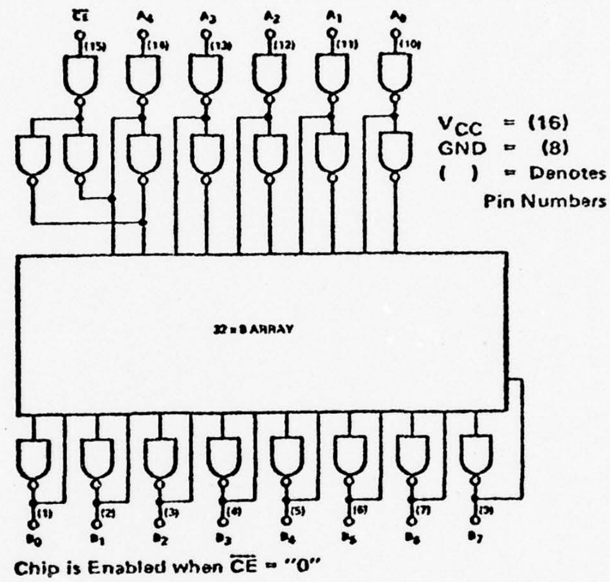


Figure A-1. 8223 Diagram

The table of values programmed into the cosine ROM pair are listed in Table A-1. The entries are in twos complement form with the left most bit serving as the sign. The right most bit is the least significant bit.

Table A. Bit patterns for cosine ROM's

Address	ROM A								ROM B							
(octal)	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
00	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1
01	0	1	1	1	1	1	1	0	1	0	0	0	0	0	1	0
02	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1	1
03	0	1	1	1	1	0	1	0	1	0	0	0	0	1	1	0
04	0	1	1	1	0	1	0	1	1	0	0	0	1	0	1	1
05	0	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0
06	0	1	1	0	1	0	1	0	1	0	0	1	0	1	1	0
07	0	1	1	0	0	0	1	0	1	0	0	1	1	1	1	0
10	0	1	0	1	1	0	1	0	1	0	1	0	0	1	1	0
11	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1
12	0	1	0	0	0	1	1	1	1	0	1	1	1	0	0	1
13	0	0	1	1	1	1	0	0	1	1	0	0	0	1	0	0
14	0	0	1	1	0	0	0	1	1	1	0	0	1	1	1	1
15	0	0	1	0	0	1	0	1	1	1	0	1	1	0	1	1
16	0	0	0	1	1	0	0	1	1	1	1	0	0	1	1	1
17	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	1	1	1	1	0	1	0	0	0	0	0	0	1	1	0	0
22	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1
23	1	1	0	1	1	0	1	1	0	0	1	0	0	1	0	1
24	1	1	0	0	1	1	1	1	0	0	1	1	0	0	0	1
25	1	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0
26	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1	1
27	1	0	1	0	1	1	1	1	0	1	0	1	0	0	0	1
30	1	0	1	0	0	1	1	0	0	1	0	1	1	0	1	0
31	1	0	0	1	1	1	1	0	0	1	1	0	0	0	1	0
32	1	0	0	1	0	1	1	0	0	1	1	0	1	0	1	0
33	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0
34	1	0	0	0	1	0	1	1	0	1	1	1	0	1	0	1
35	1	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0
36	1	0	0	0	0	0	1	1	0	1	1	1	1	1	0	1
37	1	0	0	0	0	0	1	0	0	1	1	1	1	1	1	0

APPENDIX B

Sequence ROM

The sequence control ROM is a single 8-bit by 32-word Signetics type 8223 or 82S23 integrated circuit. The same conventions used with the cosine ROM described in Appendix A are followed with this ROM.

Bit BØ is used to control the generation of the digit which is used for pulse modulation. This signal is also made available as the P-SYNC signal.

Bit B1 is used to represent the desired binary sequence.

Bits B2 through B6 are used to select the address of the next 8-bit word to be read from the memory. This approach eliminates the need for a variable modulus counter for use as an address register. Bit B2 corresponds to the least significant bit in the address and B6 corresponds to the most significant bit. It is useful to place one value of the sequence being generated into location Ø so that unprogrammed locations (which contain "zeros") automatically allow proper start-up.

Bit B7 is not currently used. However, if the sequence ROM is extended to 64 words, this bit will be used in generating addresses.

APPENDIX C

Parts List

1	Wirewrap panel AUGAT 8136-PG21-90
1	Optima Enclosure E-061110MFT (Beige with bronze trim)
1	Optima Chassis CH01110 (3/4 inch)
1	EECO Thumbwheel Switch 5R197608G
1	EECO Thumbwheel Switch 2R197618G
1	EECO Thumbwheel Switch 3R197612G
1	AC/DC Power Supply OEM 5N3-1
1	AC/DC Power Supply PCMD0.2
1	AC/DC Power Supply Socket SB2
2	Datel D/A Converters DAC-29-8B
1	Rotron Sprite Fan SU2A1
1	Rotron Fan Guard 476143
2	Centralab Rotary Switches PSA-211
1	Molex Connector 03-09-1091
6	Molex Female Contacts 02-09-1143
1	Molex Connector 03-09-2091
6	Molex Male Contacts 02-09-2103
1	AMP Mate-N-Lock Connector 1-480273
1	AMP Mate-N-Lock Connector 1-480276
6	AMP Female Contacts 60617-4
6	AMP Male Contacts 60618-4
4	3M Connectors 3399-1
7	BNC Connectors UG-1094/U
1	Potentiometer Ohmite AB-CLU-5021
1	SPST Toggle Switch JBT 138-ST42A
3	Ft. woven 26 Conductor Cable T-13TP 2807UL-1568N
7	BNC Ground Wings
1	Cinch Barrier Strip 14-5-140
1	Light Duty Three Wire Power Cord and Plug
1	Fuse Holder and Fuse, 1/2 A
7	Diodes 1N4154
10	Fairchild LED's FLV110
10	Fairchild LED Bezels FLS010
1	Signetics op amp NE531V
4	Beckman 898-1-R1K Resistor Networks
5	7402 DIP TTL Integrated Circuits
1	7404
2	7407
2	7408
1	7411
1	7420
1	7421
2	7425
2	7432
1	7437
3	7474
5	7486
1	74123
1	74132

1	74157
3	74174
3	74192
4	74193
2	75452
5	82S23 Signetics ROMs
4	AUGAT Adapter Plugs 616-CG1
1	0.05 mF 20v Disc Ceramic Capacitor
1	100 pF Disc Ceramic Capacitor
2	30 pF Disc Ceramic Capacitor
5	1k 5% 1/4 W Resistors
1	3.9k 5% 1/4 W Resistors
6	4.7k " " "
1	10k " " "
1	39k " " "
1	47k " " "
1	2.2 mF 50v Monolythic cap Centralab CY30C225M

APPENDIX D

Cable Wiring for BCSG-76

Connector BJ1

Pin	Signal	Panel Connection
1	CD0+	cycles/digit, LSIG digit 1
2	CD1+	cycles/digit, LSIG digit 2
3	CD2+	cycles/digit, LSIG digit 4
4	CD3+	cycles/digit, LSIG digit 8
5	CD4+	cycles/digit, MID digit 1
6	CD5+	cycles/digit, MID digit 2
7	CD6+	cycles/digit, MID digit 4
8	CD7+	cycles/digit, MID digit 8
9	CD8+	cycles/digit, MSIG digit 1
10	CD9+	cycles/digit, MSIG digit 2
11	CD10+	cycles/digit, MSIG digit 4
12	CD11+	cycles/digit, MSIG digit 8
13	ground	RDR output BNC ground
14	RSEL-	seq sw ROM position
15	SAMMOD-	modulation sw AM position
16	SPHS-	modulation sw PHS position
17	SCAR-	modulation sw CAR position
18	SPULSE-	modulation sw PLS position
19	AUG+	seq sw LM position
20	ground	cycles/digit, MSIG digit G
21	ground	cycles/digit, MID digit G
22	ground	cycles/digit, LSIG digit G
23	ground	selector on modulation sw
24	ground	selector on seq sw
25	ground	
26	RDRDAC+	RDR output BNC signal

On the cycles/digit switches connect the C terminals to the G terminals. Buss the G terminals together.

Wire the LED's associated with the modulation and the seq selector switches individually to +5 volts thru 390 ohm resistors. Connect the other side to the same lugs as used to select the desired option.

Connector BJ2

Pin	Signal	Panel Connection
1	F1-	sequence law, 1st digit 2
2	F2-	sequence law, 1st digit 4
3	F3-	sequence law, 2nd digit 1
4	F4-	sequence law, 2nd digit 2
5	F5-	sequence law, 2nd digit 4
6	F6-	sequence law, 3rd digit 1
7	DSYNC+	D-SYNC output BNC signal
8	PSYNC+	P-SYNC output BNC signal
9	F1OUT-	F output BNC signal
10	F4OUT-	4F output BNC signal
11	F11-	sequence law, 4th digit 4
12	F12-	sequence law, 5th digit 1
13	F13-	sequence law, 5th digit 2
14	F14-	sequence law, 5th digit 4
15	ground	
16	F7-	sequence law, 3rd digit 2
17	F8-	sequence law, 3rd digit 4
18	F9-	sequence law, 4th digit 1
19	F10-	sequence law, 4th digit 2
20	ground	D-SYNC output BNC ground
21	ground	P-SYNC output BNC ground
22	ground	F output BNC ground
23	ground	4F output BNC ground
24	ground	sequence law switch 5 G
25		
26		

Sequence law switch 1 is the least significant digit. Switch 5 is the most significant digit.

Connect pin C to pin G on all sequence law switches.

Buss together pin G on the sequence law switches.

Connector CJ1

Pin	Signal	Panel Connection
1	CLKIN+	64F input BNC signal
2	PANPOT+	THRESH pot clkwise end
3	PANPOT-	THRESH pot ctrclk end
4	PANCEN+	THRESH pot wiper
5		
6	PHSØ+	phase offset, LSIG digit 1
7	PHS1+	phase offset, LSIG digit 2
8	PHS2+	phase offset, LSIG digit 4
9	PHS3+	phase offset, MSIG digit 1
1Ø	PHS4+	phase offset, MSIG digit 2
11	PHS5+	phase offset, MSIG digit 4
12	AOUT+	TP tip jack signal
13	SEQDAC+	SEQ output BNC signal
14	CLKGND+	64F input BNC ground
15	CLKGND+	64F input BNC ground
16	CLKGND+	64F input BNC ground
17	CLKGND+	64F input BNC ground
18	SIGOFF-	no connection
19		
2Ø	ground	phase offset, MSIG digit G
21	ground	phase offset, LSIG digit G
22	ground	
23	ground	
24	ground	
25	ground	64F input BNC ground
26	ground	SEQ output BNC ground

Connect C to G on the phase offset switches.

Buss the G pins on the phase offset switches together.

Connector CJ2

Pin	Signal	Connection
2Ø	+15V	+15 volts power
21	+15V	+15 volts power
22	ground	+15 and -15 ground connection
23	-15V	-15 volts power
24	-15V	-15 volts power

Mate-N-Lock and Molex Connectors

Mate-N-Lock Power Connector

Pin	Signal
1	AC-Neutral
2	AC-Line
3	AC-Ground
4	Fan
5	Fan
6	no connection

Molex Panel Power Connector

Pin	Signal
1	Ground
2	+5 supply
3	+15 supply
4	-15 supply
5	no connection
6	no connection
7	no connection
8	AC to switch
9	AC from switch

APPENDIX E

Diagrams and Other Information

Notes:

1) Case of 15 volt power supply must be grounded.

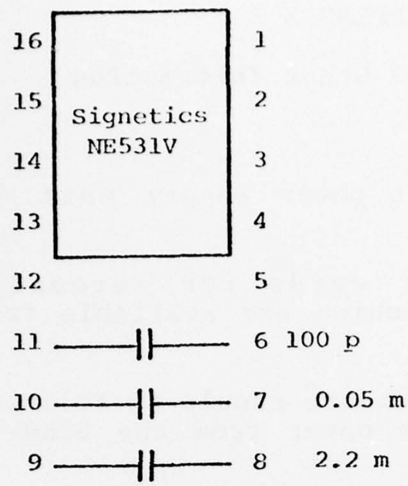
2) Wire list and/or cards for automatic Gardner-Denver machine are available from authors.

3) The following procedure should be followed in removing the cover from the BCSG-76 unit.

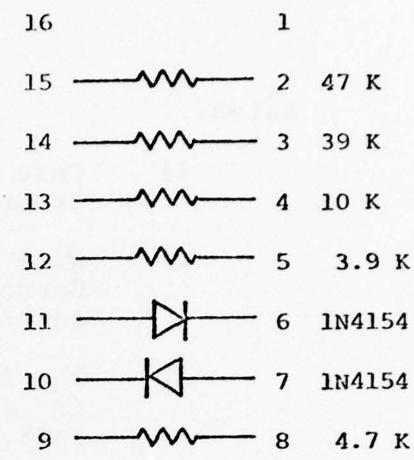
   a) On the back of the unit remove the two outermost screws (one on the left side and one on the right side).

   b) Slide the cover toward the rear to remove from the restraining groove at the front of the case.

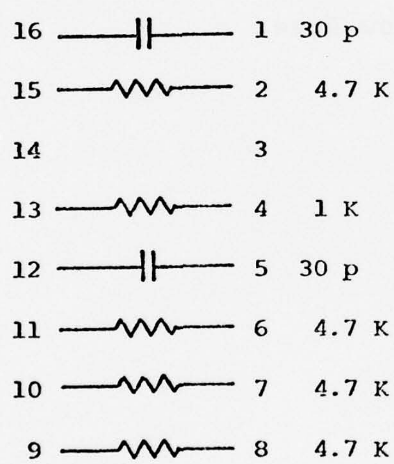
   c) The cover is now free.



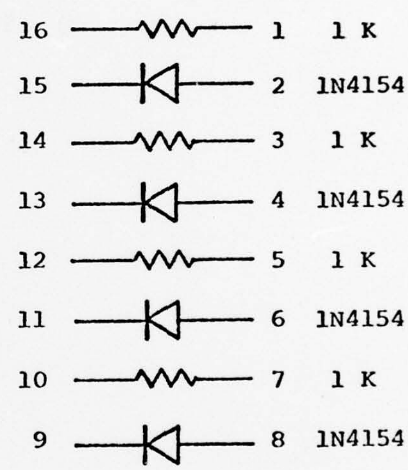
Position C01



Position C02



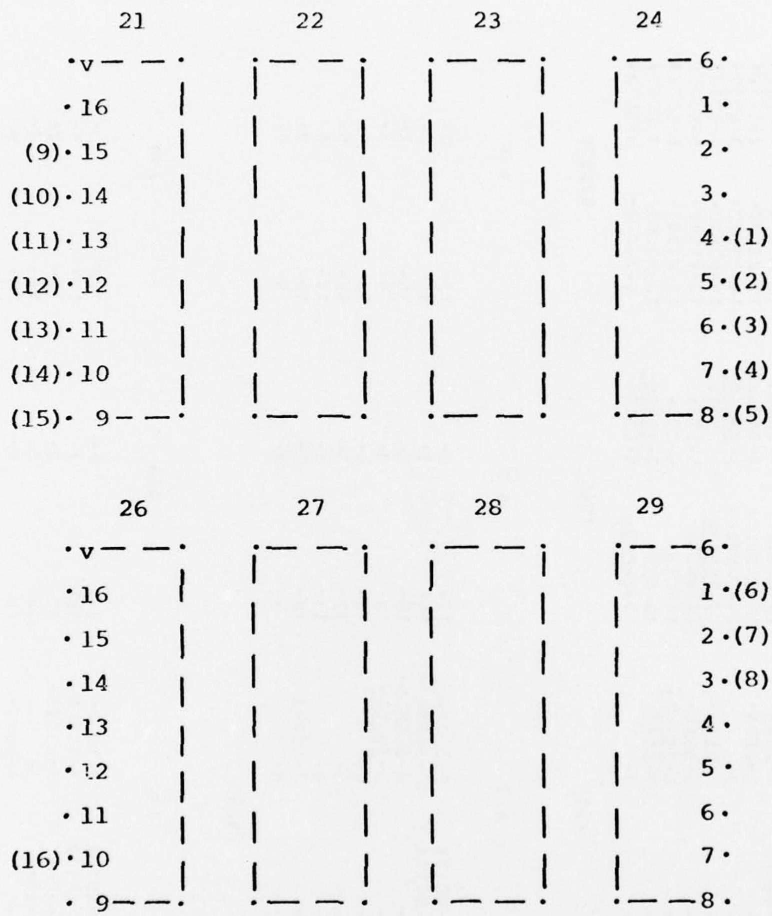
Position C08



Position A04

Parts Headers Construction

DAC Pin Assignments on Wrap Panel
(Backview)



( ) Are DAC pin numbers

A 1		A 2		A 3		A 4		A 5	
17-H006#	0-L009#	17-H007#	0-L010#	17-H008#	0-L011#	17-H009#	0-L012#	17-	0-
16-H006#	1-SDIG-	16-H007#	1-Z14-	16-H008#	1-SRCLK-	16-DSYNC+	1-H009#	16-	1-
15-	2-GDIG+	15-	2-ZERA+	15-PLSHLD-	2-SRCLK-	15-DSYNC+	2-L012#	15-	2-
14-	3-ZERO+	14-	3-	14-PLSHLD-	3-DSYNC+	14-PSYNC+	3-H009#	14-	3-
13-	4-GFB2+	13-	4-ZERB+	13-PSYNC+	4-L011#	13-PSYNC+	4-L012#	13-	4-
12-GFB1+	5-F2-	12-	5-ZERC+	12-H008#	5-CT5+	12-F1OUT-	5-H009#	12-	5-
11-SDIG-	6-SDIG-	11-	6-NEARZ+	11-CT3+	6-CT5+	11-F1OUT-	6-L012#	11-	6-
10-F1-	7-L009#	10-	7-L010#	10-CT3+	7-F1OUT-	10-F4OUT-	7-H009#	10-	7-
9-	8-	9-	8-	9-F4OUT-	8-L011#	9-F4OUT-	8-L012#	9-	8-
7402		7421		75452		HEADER			

A 6		A 7		A 8		A 9		A10	
17-H010#	0-L013#	17-H011#	0-L014#	17-	0-	17-	0-	17-	0-
16-H010#	1-SDIG-	16-H011#	1-SAMMOD-	16-	1-	16-	1-	16-	1-
15-Z1+	2-SDIG-	15-	2-DIGHLD-	15-	2-	15-	2-	15-	2-
14-NEARZ+	3-BSDIG-	14-	3-SLDIG-	14-	3-	14-	3-	14-	3-
13-SPLS+	4-Z1+	13-	4-	13-	4-	13-	4-	13-	4-
12-NEARZ+	5-DOPF-	12-	5-	12-	5-	12-	5-	12-	5-
11-Z1-	6-GDIG+	11-	6-	11-	6-	11-	6-	11-	6-
10-ZERO+	7-L013#	10-	7-L014#	10-	7-	10-	7-	10-	7-
9-	8-	9-	8-	9-	8-	9-	8-	9-	8-
7408		7432							

A11		A12		A13		A14		A15	
17-H012#	0-L015#	17-H013#	0-L016#	17-	0-	17-	0-	17-	0-
16-H012#	1-RSEL-	16-H013#	1-SLPLS-	16-	1-	16-	1-	16-	1-
15-L015#	2-RDIG+	15-AUG+	2-SLDIG-	15-	2-	15-	2-	15-	2-
14-	3-SDIG+	14-Z1+	3-	14-	3-	14-	3-	14-	3-
13-	4-VDIGIT+	13-	4-SPHS-	13-	4-	13-	4-	13-	4-
12-	5-RPLS+	12-NEARZ+	5-SCAR-	12-	5-	12-	5-	12-	5-
11-	6-SPLS+	11-NEARZ+	6-SPCOS+	11-	6-	11-	6-	11-	6-
10-	7-VPULSE+	10-DOFF-	7-L016#	10-	7-	10-	7-	10-	7-
9-	8-L015#	9-	8-	9-	8-	9-	8-	9-	8-
74157		7420							

```
            A16                   A17                   A18                   A19                   A20

17-H002#     0-L001#    17-          0-        17-         0-        17-         0-        17-         0-
16-H002#     1-L001#    16-          1-        16-         1-        16-         1-        16-         1-
15-L001#     2-L001#    15-          2-        15-         2-        15-         2-        15-         2-
14-L001#     3-H001#    14-          3-        14-         3-        14-         3-        14-         3-
13-H005#     4-L001#    13-          4-        13-         4-        13-         4-        13-         4-
12-L001#     5-L001#    12-          5-        12-         5-        12-         5-        12-         5-
11-L001#     6-H003#    11-          6-        11-         6-        11-         6-        11-         6-
10-H004#     7-L001#    10-          7-        10-         7-        10-         7-        10-         7-
 9-          8-          9-          8-         9-         8-         9-         8-         9-         8-

          7437

            A21                   A22                   A23                   A24                   A25

17-          0-         17-          0-        17-         0-        17-         0-        17-         0-
16-          1-         16-          1-        16-         1-        16-         1-        16-         1-
15-          2-         15-          2-        15-         2-        15-         2-        15-         2-
14-          3-         14-          3-        14-         3-        14-         3-        14-         3-
13-          4-         13-          4-        13-         4-        13-         4-        13-         4-
12-          5-         12-          5-        12-         5-        12-         5-        12-         5-
11-          6-         11-          6-        11-         6-        11-         6-        11-         6-
10-          7-         10-          7-        10-         7-        10-         7-        10-         7-
 9-          8-          9-          8-         9-         8-         9-         8-         9-         8-

            A26                   A27                   A28                   A29                   A30

17-          0-         17-          0-        17-         0-        17-         0-        17-         0-
16-          1-         16-          1-        16-         1-        16-         1-        16-         1-
15-          2-         15-          2-        15-         2-        15-         2-        15-         2-
14-          3-         14-          3-        14-         3-        14-         3-        14-         3-
13-          4-         13-          4-        13-         4-        13-         4-        13-         4-
12-          5-         12-          5-        12-         5-        12-         5-        12-         5-
11-          6-         11-          6-        11-         6-        11-         6-        11-         6-
10-          7-         10-          7-        10-         7-        10-         7-        10-         7-
 9-          8-          9-          8-         9-         8-         9-         8-         9-         8-
```

AJ1	AJ2
1-	1-
2-	2-
3-	3-
4-	4-
5-	5-
6-	6-
7-	7-
8-	8-
9-	9-
10-	10-
11-	11-
12-	12-
13-	13-
14-	14-
15-	15-
16-	16-
17-	17-
18-	18-
19-	19-
20-	20-
21-	21-
22-	22-
23-	23-
24-	24-
25-	25-
26-	26-

B 1

17-H014#	0-L017#
16-H014#	1-CD1+
15-CD0+	2-
14-L017#	3-
13-CB1+	4-CYCLK+
12-CC1+	5-H005#
11-SRCLK-	6-
10-CD2+	7-
9-CD3+	8-L017#

74192

B 2

17-H015#	0-L005#
16-H015#	1-CD0+
15-SIGOFF-	2-CD1+
14-SAMMOD-	3-CD2+
13-SPULSE-	4-CD3+
12-CD11+	5-CD4+
11-CD10+	6-CD5+
10-CD9+	7-CD6+
9-CD8+	8-CD7+

RESNET

B 3

17-H016#	0-L003#
16-H016#	1-FB14+
15-GFB11+	2-F14-
14-BSDIG-	3-BSDIG-
13-F11-	4-GFB13+
12-GFB12+	5-F13-
11-BSDIG-	6-BSDIG-
10-F12-	7-L003#
9-	8-

7402

B 4

17-H017#	0-L004#
16-H017#	1-GFB10+
15-GFB7+	2-F10-
14-BSDIG-	3-BSDIG-
13-F7-	4-GFB9+
12-GFB8+	5-F9-
11-BSDIG-	6-BSDIG-
10-F8-	7-L004#
9-	8-

7402

B 5

17-H018#	0-L002#
16-H018#	1-GFB6+
15-GFB3+	2-F6-
14-SDIG-	3-SDIG-
13-F3-	4-GFB5+
12-GFB4+	5-F5-
11-SDIG-	6-SDIG-
10-F4-	7-L002#
9-	8-

7402

B 6

17-H019#	0-L018#
16-H019#	1-CD5+
15-CD4+	2-
14-L018#	3-
13-CB2+	4-CB1+
12-CC2+	5-CC1+
11-SRCLK-	6-
10-CD6+	7-
9-CD7+	8-L018#

74192

B 7

17-H020#	0-
16-H020#	1-F14-
15-RSSL-	2-F13-
14-F1-	3-F12-
13-F2-	4-F11-
12-F3-	5-F10-
11-F4-	6-F9-
10-F5-	7-F8-
9-F6-	8-F7-

RESNET

B 8

17-H021#	0-L019#
16-H021#	1-Z12+
15-GFB8+	2-GFB11+
14-Z9+	3-FB11+
13-FB8+	4-Z11+
12-GFB9+	5-GFB10+
11-Z10+	6-FB10+
10-FB9+	7-L019#
9-	8-

7486

B 9

17-H022#	0-L020#
16-H022#	1-Z8+
15-GFB4+	2-GFB7+
14-Z5+	3-FB7+
13-FB4+	4-Z7+
12-GFB5+	5-GFB6+
11-Z6+	6-FB6+
10-FB5+	7-L020#
9-	8-

7486

B10

17-H023#	0-L021#
16-H023#	1-Z4+
15-	2-GFB3+
14-	3-FB3+
13-	4-Z3+
12-GFB1+	5-GFB2+
11-Z2+	6-FB2+
10-FB1+	7-L021#
9-	8-

7486

B11

17-H024#	0-L022#
16-H024#	1-CD9+
15-CD8+	2-
14-L022#	3-
13-CYCTIC-	4-CB2+
12-	5-CC2+
11-SRCLK-	6-
10-CD10+	7-
9-CD11+	8-L022#

74192

B12

17-H025#	0-L023#
16-H025#	1-Z9+
15-Z2+	2-Z8+
14-Z3+	3-H005#
13-H005#	4-Z7+
12-Z4+	5-Z6+
11-Z5+	6-ZERB+
10-ZERC+	7-L023#
9-	8-

7425

B13

17-H026#	0-L024#
16-H026#	1-H005#
15-H005#	2-FB14+
14-FB13+	3-SRCLK+
13-SRCLK+	4-H005#
12-H005#	5-Z14+
11-Z13+	6-Z14-
10-	7-L024#
9-	8-

7474

B14

17-H027#	0-L025#
16-H027#	1-H005#
15-Z7+	2-Z12+
14-FB7+	3-FB12+
13-FB8+	4-FB11+
12-Z8+	5-Z11+
11-FB9+	6-FB10+
10-Z9+	7-Z10+
9-SRCLK+	8-L025#

74174

B15

17-H028#	0-L026#
16-H028#	1-H005#
15-Z1+	2-Z6+
14-FB1+	3-FB6+
13-FB2+	4-FB5+
12-Z2+	5-Z5+
11-FB3+	6-FB4+
10-Z3+	7-Z4+
9-SRCLK+	8-L026#

74174

B16

17-H029#	0-L027#
16-H029#	1-
15-	2-CT5+
14-L027#	3-CT4+
13-	4-RDBOR+
12-	5-RDCAR+
11-H005#	6-
10-	7-
9-	8-L027#

74193

B17

17-H030#	0-L028#
16-H030#	1-
15-	2-CT1+
14-L028#	3-CT0+
13-RDBOR+	4-H005#
12-RDCAR+	5-BF64+
11-H005#	6-CT2+
10-	7-CT3+
9-	8-L028#

74193

B18

17-H031#	0-
16-H031#	1-RR7+
15-ADR4+	2-RR6+
14-ADR3+	3-RR5+
13-ADR2+	4-RR4+
12-ADR1+	5-RR3+
11-ADR0+	6-RR2+
10-SCAR-	7-RR1+
9-SPHS-	8-RR0+

RESNET

B19

17-H032#	0-L029#
16-H032#	1-H005#
15-	2-L0+
14-	3-ADR0+
13-ADR4+	4-ADR1+
12-L4+	5-L1+
11-ADR3+	6-ADR2+
10-L3+	7-L2+
9-SRCLK+	8-L029#

74174

B20

17-H033#	0-L030#
16-H033#	1-RPLS+
15-L030#	2-RDIG+
14-L4+	3-ADR0+
13-L3+	4-ADR1+
12-L2+	5-ADR2+
11-L1+	6-ADR3+
10-L0+	7-ADR4+
9-	8-L030#

8223

B21

17-	0-L031#
16-	1-
15-P15V	2-
14-M15V	3-
13-L031#	4-
12-RDRDAC+	5-
11-OFSETB	6-
10-	7-
9-OFSETB	8-

HEADER

B22

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

B23

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

B24

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-RR7+
12-	5-RR6+
11-	6-RR5+
10-	7-RR4+
9-	8-RR3+

HEADER

B25

17-H034#	0-L032#
16-H034#	1-RR0+
15-CT5-	2-RR1+
14-CT4+	3-RR2+
13-CT3+	4-RR3+
12-CT2+	5-RR4+
11-CT1+	6-RR5+
10-CT0+	7-RR6+
9-RR7+	8-L032#

8223

B26

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

HEADER

B27

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

B28

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

B29

17-	0-
16-	1-RR2+
15-	2-RR1+
14-	3-RR0+
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

HEADER

B30

17-H035#	0-L033#
16-H035#	1-RR0+
15-CT5+	2-RR1+
14-CT4+	3-RR2+
13-CT3+	4-RR3+
12-CT2+	5-RR4+
11-CT1+	6-RR5+
10-CT0+	7-RR6+
9-RR7+	8-L033#

8223

BJ1	BJ2
1-CD0+	1-F1-
2-CD1+	2-F2-
3-CD2+	3-F3-
4-CD3+	4-F4-
5-CD4+	5-F5-
6-CD5+	6-F6-
7-CD6+	7-DSYNC+
8-CD7+	8-PSYNC+
9-CD8+	9-F1OUT-
10-CD9+	10-F4OUT-
11-CD10+	11-F11-
12-CD11+	12-F12-
13-L002#	13-F13-
14-RSEL-	14-F14-
15-SAMMOD-	15-L005#
16-SPHS-	16-F7-
17-SCAR-	17-F8-
18-SPULSE-	18-F9-
19-AUG+	19-F10-
20-L003#	20-L003#
21-L003#	21-L003#
22-L004#	22-L004#
23-L004#	23-L004#
24-L004#	24-L004#
25-L004#	25-
26-RDRDAC+	26-

C 1

17-	0-
16-COMP+	1-
15-P15V	2-AIN-
14-AOUT+	3-AIN+
13-	4-M15V
12-	5-
11-AOUT+	6-COMP+
10-COMP+	7-CLKGND+
9-CLKR+	8-CLKIN+

HEADER

C 2

17-H036#	0-L034#
16-	1-
15-AIN-	2-AOUT+
14-AIN-	3-PANCEN+
13-AIN-	4-CLKR+
12-AIN+	5-CLKGND+
11-STF64+	6-AOUT+
10-STF64+	7-L034#
9-STF64+	8-H036#

HEADER

C 3

17-H037#	0-L006#
16-H037#	1-STF64+
15-	2-STF64+
14-	3-F64+
13-	4-
12-	5-
11-	6-
10-	7-L006#
9-	8-

74132

C 4

17-H038#	0-L007#
16-H038#	1-F64+
15-PLSHLD-	2-PHSEL+
14-SPULSE-	3-DF64+
13-SLPLS-	4-F64+
12-SPHS-	5-PHSEL-
11-PHDIG+	6-UF64+
10-PHSEL+	7-L007#
9-	8-

7432

C 5

17-H039#	0-L008#
16-H039#	1-H005#
15-	2-L008#
14-	3-F64+
13-	4-CYCTIC-
12-	5-SRCLK+
11-	6-SRCLK-
10-	7-L008#
9-	8-

7474

C 6

17-H040#	0-L035#
16-H040#	1-F64+
15-	2-F64+
14-	3-F64B+
13-	4-F64+
12-SIGOFF-	5-F64+
11-SPCOS+	6-BF64+
10-COSON+	7-L035#
9-	8-

7408

C 7

17-H041#	0-L036#
16-H041#	1-L036#
15-TRC+	2-DF64-
14-TC+	3-H005#
13-DF64PL+	4-
12-DF64-	5-
11-H005#	6-
10-F64B+	7-
9-L036#	8-L036#

74123

C 8

17-H042#	0-
16-TC+	1-TRC+
15-TRC+	2-H042#
14-	3-
13-AUG+	4-H042#
12-	5-
11-	6-
10-M15V	7-PANPOT-
9-P15V	8-PANPOT+

HEADER

C 9

17-H043#	0-L037#
16-H043#	1-PHSEL+
15-Z1+	2-PHSEL-
14-Z1-	3-VDIGIT+
13-CT5+	4-VDIGIT-
12-CT5-	5-PHC5+
11-SDIG-	6-PHC5-
10-SDIG+	7-L037#
9-	8-

7404

C10

17-H044#	0-L038#
16-H044#	1-PHDIG+
15-	2-SPHS-
14-	3-VDIGIT-
13-	4-PM4+
12-	5-PM4-
11-	6-PM5-
10-	7-L038#
9-	8-

7402

C11

17-H045#	0-L039#
16-H045#	1-COSON+
15-COSON+	2-COSC+
14-COS5+	3-COSON+
13-COSON+	4-COS1+
12-COS4+	5-COSON+
11-COSON+	6-COS2+
10-COS3+	7-L039#
9-	8-

7407

C12

17-H046#	0-L040#
16-H046#	1-COSON+
15-	2-COS6+
14-	3-COSON+
13-	4-COS7+
12-	5-
11-	6-
10-	7-L040#
9-	8-

7407

C13

17-H047#	0-L041#
16-H047#	1-H005#
15-H005#	2-VPULSE+
14-VDIGIT+	3-BF64+
13-BF64+	4-H005#
12-H004#	5-
11-	6-PLSHLD-
10-DIGHLD-	7-L041#
9-	8-

7474

C14

17-H048#	0-L042#
16-H048#	1-
15-	2-PHC1+
14-L042#	3-PHC0+
13-CDPH+	4-DF64+
12-CUPH+	5-UF64+
11-H004#	6-PHC2+
10-	7-PHC3+
9-	8-L042#

74193

C15

17-H049#	0-L043#
16-H049#	1-PHC0+
15-PHS3+	2-PHS0+
14-PHC3+	3-PM0-
13-PM3-	4-PHC1+
12-PHS2+	5-PHS1+
11-PHC2+	6-PM1-
10-PM2-	7-L043#
9-	8-

7486

C16

17-H050#	0-L044#
16-H050#	1-COS0+
15-PHC5-	2-COS1+
14-PHC4+	3-COS2+
13-PHC3+	4-COS3+
12-PHC2+	5-COS4+
11-PHC1+	6-COS5+
10-PHC0+	7-COS6+
9-COS7+	8-L044#

8223

C17

17-H051#	0-L045#
16-H051#	1-COS0+
15-PHC5+	2-COS1+
14-PHC4+	3-COS2+
13-PHC3+	4-COS3+
12-PHC2+	5-COS4+
11-PHC1+	6-COS5+
10-PHC0+	7-COS6+
9-COS7+	8-L045#

8223

C18

17-H052#	0-
16-H052#	1-COS0+
15-PHS5+	2-COS1+
14-PHS4+	3-COS2+
13-PHS3+	4-COS3+
12-PHS2+	5-COS4+
11-PHS1+	6-COS5+
10-PHS0+	7-COS6+
9-SPHS-	8-COS7+

RESNET

C19

17-H053#	0-L046#
16-H053#	1-
15-	2-PHC5+
14-L046#	3-PHC4+
13-	4-CDPH+
12-	5-CUPH+
11-H004#	6-
10-	7-
9-	8-L046#

74193

C20

17-H054#	0-L047#
16-H054#	1-PHC4+
15-GFB12+	2-PHS4+
14-Z13+	3-PM4-
13-FB12+	4-PHC5+
12-GFB13+	5-PHS5+
11-Z14+	6-PM5-
10-FB13+	7-L047#
9-	8-

7486

C21

17-	0-L048#
16-	1-
15-P15V	2-
14-M15V	3-
13-L048#	4-
12-SEQDAC+	5-
11-OFSETC	6-
10-	7-
9-OFSETC	8-

HEADER

C22

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

C23

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

C24

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-COS7+
12-	5-COS6+
11-	6-COS5+
10-	7-COS4+
9-	8-COS3+

HEADER

C25

17-H055#	0-L049#
16-H055#	1-PM0-
15-Z10+	2-PM1-
14-Z11+	3-H004#
13-H004#	4-PM2-
12-Z12+	5-PM3-
11-Z13+	6-PMA+
10-ZERA+	7-L049#
9-	8-

7425

C26

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

HEADER

C27

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

C28

17-	0-
16-	1-
15-	2-
14-	3-
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

C29

17-	0-
16-	1-COS2+
15-	2-COS1+
14-	3-COS0+
13-	4-
12-	5-
11-	6-
10-	7-
9-	8-

HEADER

C30

17-H056#	0-L050#
16-H056#	1-DF64PL+
15-PMB+	2-PMA+
14-CYCLK+	3-
13-	4-
12-	5-
11-	6-
10-	7-L050#
9-	8-

7411

CJ1	CJ2
1-CLKIN+	1-
2-PANPOT+	2-
3-PANPOT-	3-
4-PANCEN+	4-
5-	5-
6-PHS0+	6-
7-PHS1+	7-
8-PHS2+	8-
9-PHS3+	9-
10-PHS4+	10-
11-PHS5+	11-
12-AOUT+	12-
13-SEQDAC+	13-
14-CLKGND+	14-
15-CLKGND+	15-
16-CLKGND+	16-
17-CLKGND+	17-
18-SIGOFF-	18-
19-	19-
20-L006#	20-P15V
21-L006#	21-P15V
22-L007#	22-L007#
23-L007#	23-M15V
24-L007#	24-M15V
25-L007#	25-L007#
26-L008#	26-L008#

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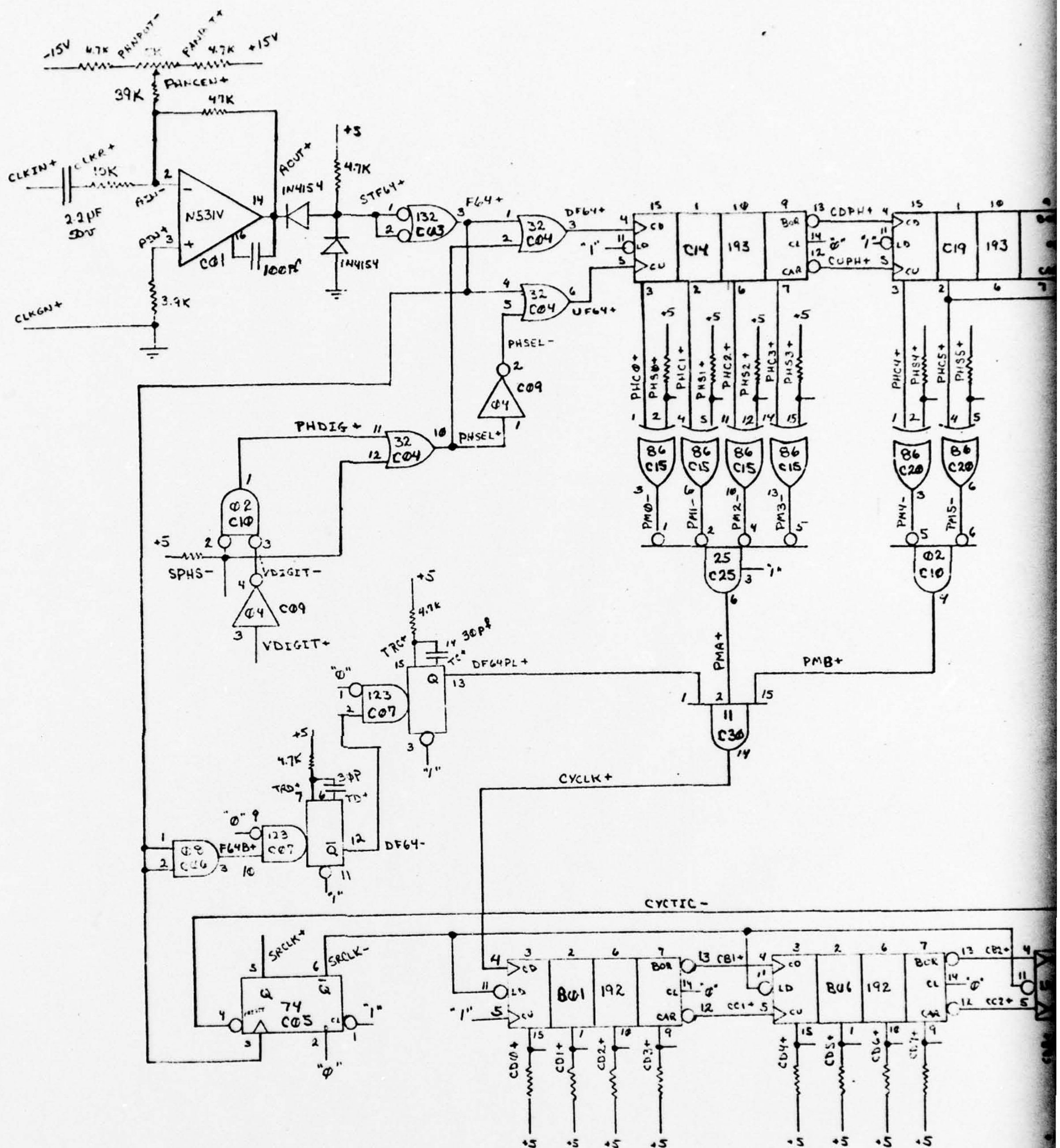
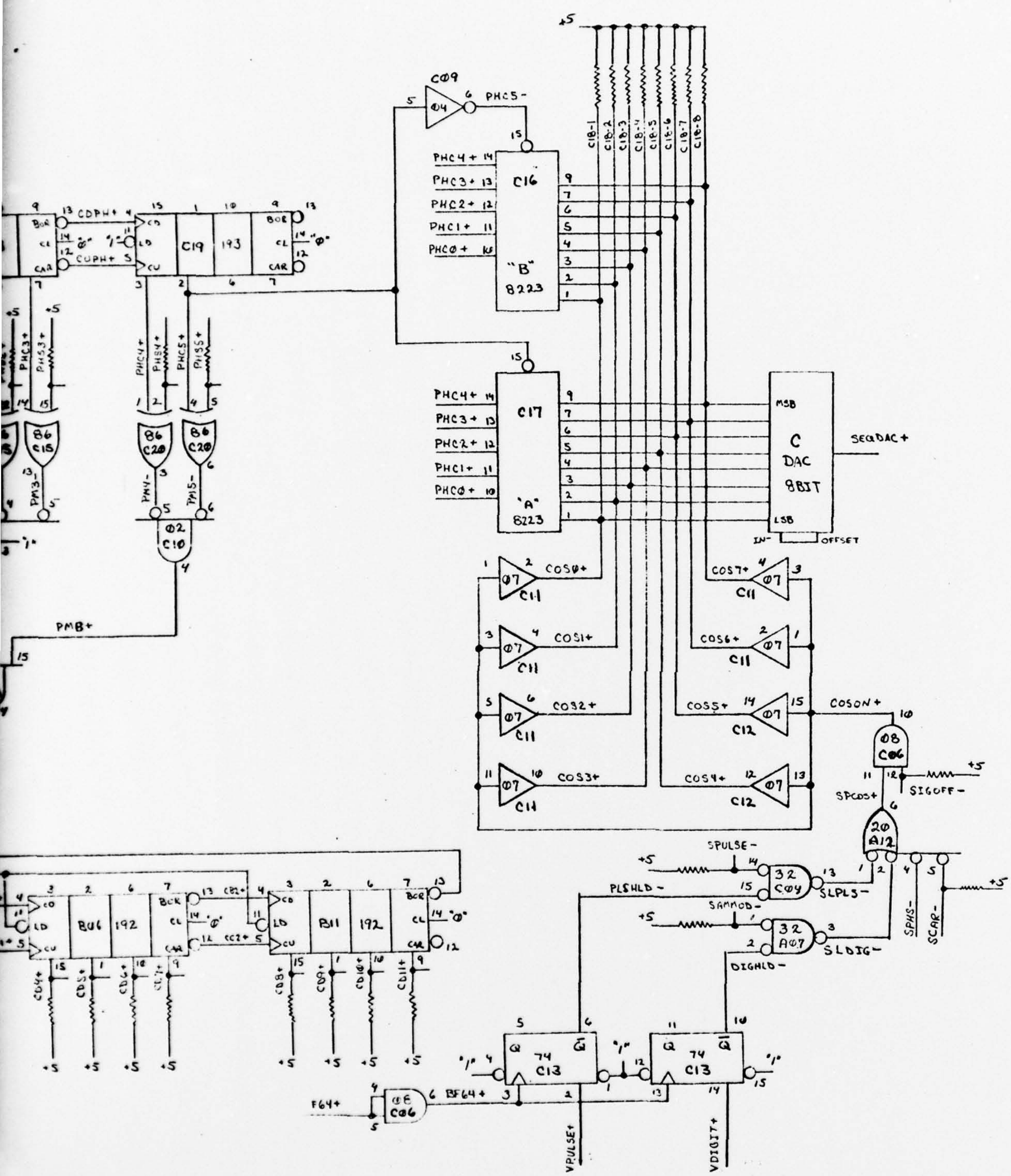


UNLABLED RESISTORS ARE 1K RESNETS
(Φ) = GROUND

KM
6/76

2



+5
C09
PHC5-
C16
"B"
8223
PHC4+
PHC3+
PHC2+
PHC1+
PHC0+
C17
"A"
8223
C18-1
C18-2
C18-3
C18-4
C18-5
C18-6
C18-7
C18-8
C
DAC
8BIT
MSB
LSB
OFFSET
SEQDAC+
C19
193
CDPH+
CUPH+
PMB+
C10
C15
C20
COS0+
COS1+
COS2+
COS3+
COS4+
COS5+
COS6+
COS7+
C11
C12
COSON+
C06
SIGOFF-
SPCOS+
A12
SPULSE-
SLPLS-
PLSHLD-
SAMMOD-
SLDIG-
DIGHLD-
SPHS-
SCAR-
B06
B11
192
CD4+
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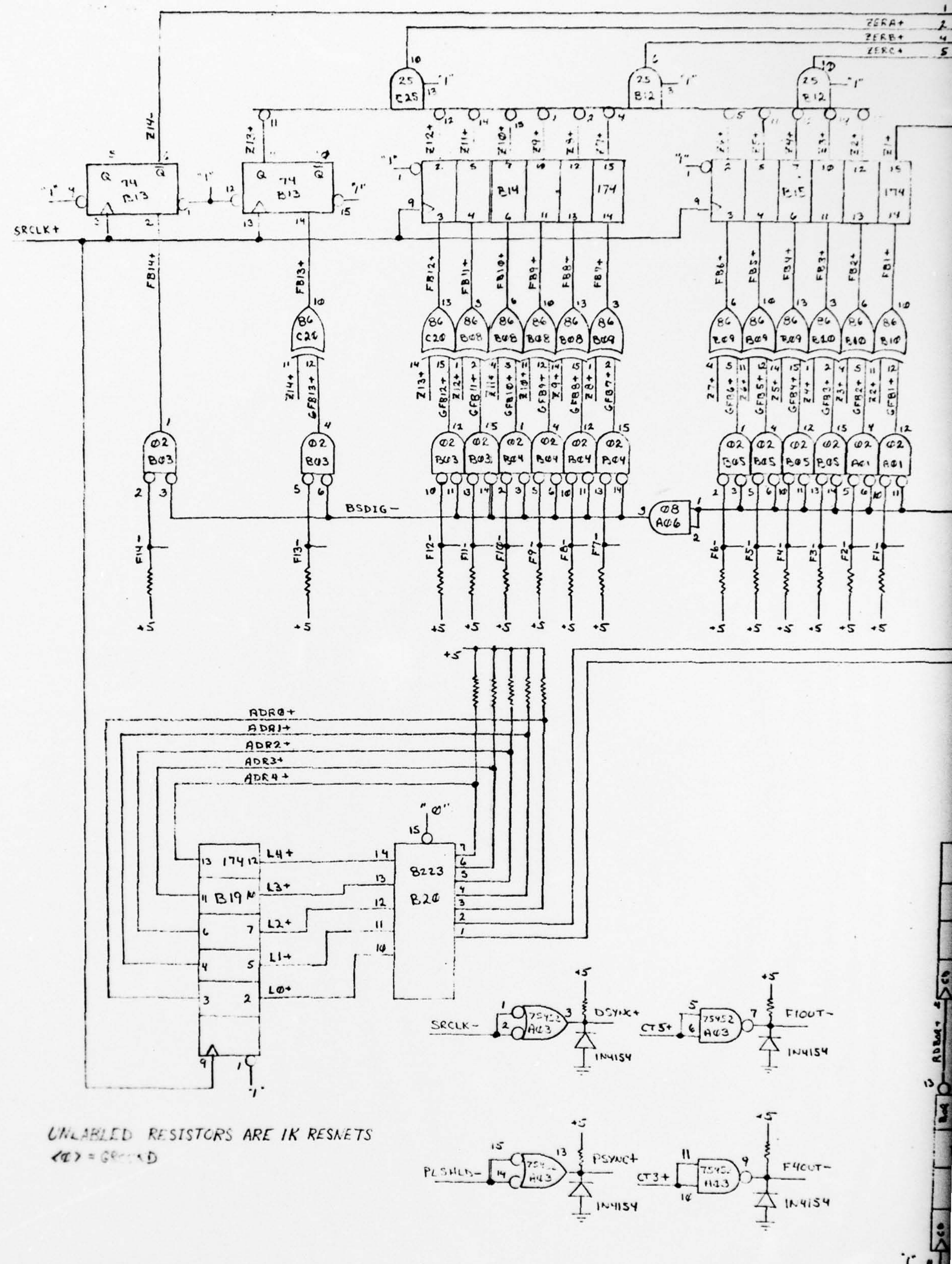
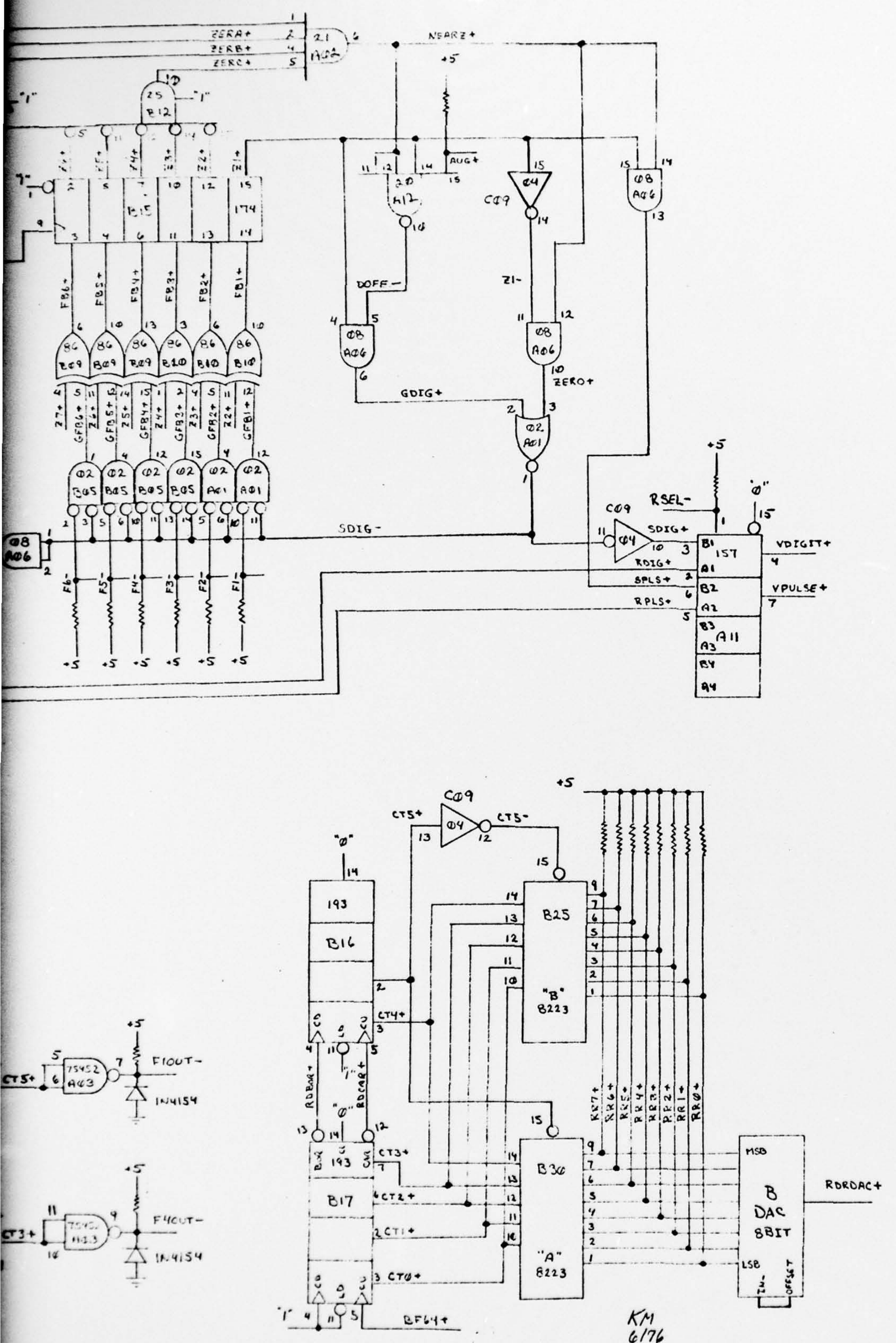
BF64+
VPULSE+
VDIGIT+



UNLABLED RESISTORS ARE 1K RESNETS
<Φ> = GROUND

2



ZERA+
ZERB+
ZERC+
NEARZ+
+5
AUG+
DOFF-
Z1-
GDIG+
ZERO+
SDIG-
RSEL-
SDIG+
RDIG+
SPLS+
RPLS+
VDIGIT+
VPULSE+
157
A11
FB6+
FB5+
FB4+
FB3+
FB2+
FB1+
193
B16
B17
B25
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8223
B30
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8223
CT5+
CT5-
CT4+
CT3+
CT2+
CT1+
CT0+
RDBOR+
RDCAR+
BF64+
F1OUT-
F4OUT-
1N4154
MSB
LSB
B
DAC
8BIT
OFFSET
RDRDAC+
KM
6/76